

TPMC630 Reconfigurable FPGA with 64 TTL I/O / 32 Diff. I/O

Application Information

The TPMC630 is a standard single-width 32 bit PMC module providing a user configurable FPGA with 300,000 system gates. All local signals from the PCI controller are routed to the FPGA.

The TPMC630-10 has 64 ESD-protected TTL lines, the TPMC630-11 provides 32 differential I/O lines using EIA-422 / EIA-485 compatible, ESD-protected line transceivers. The TPMC630-12 provides 32 TTL and 16 differential I/Os. All lines are individually programmable as input, output or tri-state. The receivers are always enabled, which allows determining the state of each I/O line at any time. This can be used as read back function for lines configured as outputs. Each TTL I/O line has a pull-up resistor. The pull-up voltage is selectable to be either +3.3V or +5V. The differential I/O lines are terminated by 120Ω resistors.

The FPGA is configured by a serial Flash. The Flash device is in-system programmable via driver software over the PCI bus. An in-circuit debugging option is available via an optionally mountable JTAG header (on the backside of the board) for readback and real-time debugging of the FPGA design (using Xilinx "ChipScope").

A programmable clock generator supplies up to six different clock frequencies between 200 kHz and 166 MHz. All outputs are available at the FPGA, one clock source is in addition used as the local clock signal for the PCI controller. The clock generator settings are stored in an EEPROM and can be changed by the driver software through PCI9030 GPIO pins.

The configuration EEPROM of the PCI controller can also be modified by the driver software, to adapt address spaces etc.

User applications can be developed using the design software ISE WebPACK which can be downloaded free of charge from www.xilinx.com.

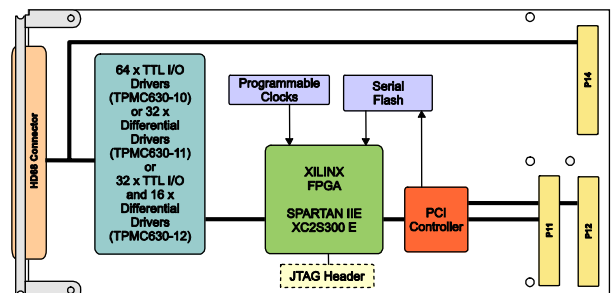
The TPMC630 provides front panel I/O via a HD68 SCSI-3 type connector and rear panel I/O via P14.

For First Time Users the Engineering Documentation TPMC630-ED is recommended. The Engineering Documentation includes TPMC630-DOC, schematics, data sheets / application notes of the components and well documented sample VHDL source code.

Driver support (TPMC630-SW-xx) for different operating systems is available.

Technical Information

- Standard single-width 32 bit PMC module conforming to IEEE P1386.1
- PCI 2.1 compliant interface
- Board size: 149 mm x 74 mm
- Xilinx XC2S300E-6 Spartan-II E FPGA configured by serial Flash XCF02S
- Flash device in-system programmable
- 32 bit PCI target interface by PLX PCI9030
- FPGA clock options:
 - Local clock oscillator
 - PLL programmable clock generator (200 KHz – 166 MHz), 6 clock outputs connected to FPGA
- I/O lines
 - 64 TTL I/O (-10), 32 differential I/O (-11) or 32 TTL I/O and 16 differential I/O (-12)
 - TTL signaling voltage (maximum current: +/-24 mA) or EIA-422/-485 signaling level
 - direction individually programmable
- I/O access:
 - 64 I/O lines on HD68 front connector, parallel to up to 64 I/O lines on rear connector P14
- Operating temperature: -40°C to +85°C



Order Information

TPMC630-10	64 TTL Inputs/Outputs	TPMC630-SW-12	OS-9 Software Support
TPMC630-11	32 Differential Inputs/Outputs	TPMC630-SW-32	pSOS Software Support
TPMC630-12	32 TTL Inputs/Outputs and 16 Differential Inputs/Outputs	TPMC630-SW-42	VxWorks Software Support
TPMC630-DOC	User Manual	TPMC630-SW-62	Windows NT 4.0 Software Support
TPMC630-ED	Engineering Documentation, includes TPMC630-DOC	TPMC630-SW-65	Windows XP/2000 Software Support
TA304-10	Cable Kit for modules with HD68 SCSI-3 type connector	TPMC630-SW-72	LynxOS Software Support
TPIM002-10	PIM I/O Module with HD68 SCSI-3 type connector	TPMC630-SW-82	LiNIX Software Support
TPIM002-DOC	User Manual for TPIM002-10	TPMC630-SW-92	QNX 4 Software Support
		TPMC630-SW-95	QNX 6 Software Support